REMARKS

Claims 1 and 3-9 are pending in the present application. Claim 1 is amended above and claims 2 and 10-17 are canceled above. No new matter is added by the claim amendments. Entry is respectfully requested.

The Title and the Specification stand objected to for informalities stated in the Office Action.. These informalities are believed to be cured by the amendments made to the Title and the Specification above. Removal of the objections are respectfully requested.

The drawings are objected to for informalities stated in the Office Action. These informalities are believed to be cured by the formal drawings submitted in the application on July 1, 2003. Entry of the formal drawings and removal of the objections are respectfully requested.

Claim 2 stands rejected under 35 U.S.C. 112, first paragraph. Claim 2 is canceled above and claim 1 is amended above in a manner that is believed to overcome the rejection. Removal of the rejection is respectfully requested. Specifically, the word "void" of former claim 2 is amended to state "undermined" in amended Claim 1 as filed. The specification as filed discusses that the pad 308a, 308b is formed by filling etch-stop material in the "undermined" region 221 that is formed by removing a portion of the second dielectric layer 302 at least at page 9, lines 10-23, with reference to FIGs. 3C and 3D.

Claims 1, 4, 8, and 9 stand rejected under 35 U.S.C. 102(b) as being anticipated by Havemann, et al. (U.S. Patent No. 5,661,344-hereinafter " Havemann"). Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann and Irinoda (U.S. Patent No. 5,726,499). Claims 3 and 5-7 stand rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Havemann and Nakamura, et al. (U.S. Patent No. 6,492,730).

The present invention of amended independent claim 1 is directed to a semiconductor device comprising a first dielectric layer, a second dielectric layer, a stud, a third dielectric layer, and a first pad. The first dielectric layer is formed on a substrate and the second dielectric layer is formed on the first dielectric layer. The stud is formed through the first and second dielectric layers and the third dielectric layer is formed over a top of the stud. The first pad is formed of a first etch stop material and is formed in an undermined region below the third dielectric layer remaining after removal of a portion of the second dielectric layer.

Havemann is directed to a semiconductor device (refer to Havemann FIG. 4) which comprises patterned conductors 18, a substrate encapsulating layer 32, a dielectric layer 22, a cap layer 24, a second encapsulating layer 36, a via passivation layer 30, a second conductor layer 38 and a second cap layer 42, as shown in FIG. 4. The dielectric layer 22 is formed on the substrate 10 and conductors 18. The cap layer 24 is deposited over dielectric layer 22. Vias are etched through the cap layer 24 and the dielectric layer 22, and a patterned conductor layer 38 is provided to fill in the vias. The second encapsulation layer 36 is deposited over the exposed surfaces of cap layer 24 and second conductor layer 38. The second dielectric layer 40 and second cap layer 42 are deposited sequentially over the second encapsulation layer 36. (See Havemann FIG. 4 and column 5, line 59-column 7, line 32)

Irinoda is directed to a contact structure (see FIGs. 5A-5E of Irinoda) having a depression 103 that is formed in an insulator layer 102 and a silicon nitride layer 104. A polysilicon ring 105A is formed in the depression 103 at the sides of the insulation layer 102 and silicon nitride layer 104, as shown in FIGs. 6 and 7.

It is respectfully submitted that neither Havemann nor Irinoda, nor their combination, teaches or suggests the present invention as claimed in amended independent claim 1.

Specifically, Havemann fails to teach or suggest "a first pad ... formed in a undermined region below the third dielectric layer remaining after removal of a portion of the second dielectric layer," as claimed in amended independent claim 1.

In Havemann, the second substrate encapsulation layer 36 which, according to the Office Action, is considered to be analogous to the "first pad" of the present invention of claim 1, is formed over the exposed surfaces of cap layer 24, which is considered by the Office Action to be analogous to the "second dielectric layer" of the present invention of claim 1, and over the second conductor layer 38, which is considered by the Office Action to be analogous to the "stud" of the present invention of claim 1. Assuming this to be true, then the second substrate encapsulation layer 36 of Havemann is not formed in an "undermined region below the third dielectric layer remaining after removal of a portion of the second dielectric layer," as is the "first pad" of the present invention. The feature of the "first pad" of the present invention is illustrated, for example, at FIGs 3a-3f and 4a-4f of the specification, where it can be seen that the pad is formed in an undermined region 308a which is formed by removing a portion of the second dielectric layer 302. This is in contrast with Havemann in which the second substrate encapsulation layer 36 is formed over top surfaces of the cap layer 24 and the second conductor layer 38, and not in an "undermined region" of the cap layer 24.

With respect to the rejection of former claim 2, it is submitted that Irinoda also fails to teach or suggest "a first pad of first etch stop material formed in a undermined region remaining after removal of a portion of the second dielectric layer ", as claimed in amended independent claim 1.

Irinoda is cited in the Office Action as teaching forming a dielectric pad 105A in a void of dielectric layer 102. In Irinoda, a polysilicon ring 105A, which, according to the Office Action, is considered to be analogous to the "first pad" of the present invention in claim 1, is formed at exposed edges of both insulation layer 102 and silicon nitride layer 104 which are

considered by the Office Action to be analogous to the "second dielectric layer" and the "third dielectric layer" respectively, of the present invention of claim 1. However, in the present invention of amended independent claim 1, the "first pad" is "formed in an undermined region" which is "below the third dielectric layer" that is formed by the removal of a portion of the "second dielectric layer". It can be seen in the examples of FIGs. 3c and 3d, and 4c and 4d that the pad is formed below the first etch stop layer 304 (which corresponds to the "third dielectric layer" of claim 1) and in an "undermined region" 308a, 320 which is formed by removing "a portion of the second dielectric layer" 302, as discussed in the present specification at least at page 9, lines 10-23 and at page 11, lines 7-17. In addition, the polysilicon ring 105A of Irinoda is formed of polysilicon. In contrast, the "first pad" of the present invention of the claim 1 is formed of and "etch stop material," for example, Si_3N_4, Ta_2O_5, or Al_2O_3, as stated in the specification as filed at page 7, lines 17-18.

For the reasons stated above, it is submitted that the combination of Havemann and Irinoda fails to teach or suggest the invention as set forth in amended independent claim 1, since neither Havemann, nor Irinoda, nor their combination teaches or suggests "a first pad of etch stop material formed in a undermined region below the third dielectric layer remaining after removal of a portion of the second dielectric layer." Accordingly, reconsideration of the rejection and allowance of amended independent claim 1 are respectfully requested. With regard to dependent claims 3-9, it follows that these claims should inherit the allowability of independent claim 1, from which they depend.

Claims 1-9 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,518,671. Claims 1-9 further stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of U.S. Patent No. 6,350,649. The Terminal Disclaimer filed herewith is believed to address and obviate the double patenting rejections. Removal of the rejections is therefore respectfully requested.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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